On page 19, line 36, delete "[", and delete "]".

On page 20, line 4, delete "[", and delete "]".

On page 24, line 19, delete "[", and delete "]".

On page 24, line 36, delete "(", and delete ")".

On page 27, line 25, replace "DE" with --No.--.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A bus system, comprising:

[produced by bundling several] a plurality of at least one of individual lines, [or] buses, [or] and subbuses [(see Figures 4, 5)] within at least one of a unit [of the DFP, FPGA or DPGA type] including at least one of a data flow processor (DFP), a field programmable gate array (FPGA), a dynamically programmable gate array (DPGA), and a unit having a [as well as all units having a two- or] multi-dimensional programmable cell architecture[(see Figures 1, 2, 3) by means of which multiple units can be combined and/or memories and/or peripherals can be connected (see Figure 10)], the plurality of the at least one of individual lines, buses and subbuses being bundled,

wherein the plurality of the at least one individual lines, buses and subbuses at least one of combines multiple units and connects at least one of memories and peripherals.

2. (Amended) The bus system according to claim 1, [characterized in that] wherein at least one interface [or more interfaces (Figures 6, 7) assume the function of combining] combines the lines and [create] creates the bus system.

3. (Amended) The bus system according to claim 2 [1, characterized in that] wherein at least one [or more] state machine controls the at least one interface [machines (0703/0603) control the interfaces (see Figures 6, 7)].

4. (Amended) The bus system according to claim 3, [1, characterized in that the state machine also] wherein the at least one state machine controls [the] an external bus.

9. (Amended) The bus system according to claim 1, [characterized in that there is] further comprising:

an address generator [(0610/0710) which generates] generating [the] addresses for the units to be contacted via the bus system.

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5. (Amended) The bus system according to claim 2, [1, characterized in that the interfaces use one or more internal bus systems which may comprise] wherein the at least one interface uses at least one internal bus system, the at least one internal bus system including multiple lines [(see Figures 4, 5)] for reading and writing [(see Figure 9a, I-BUS)].

6. (Amended) The bus system according to claim 2, [1, characterized in that the interfaces use one or more internal bus systems which may comprise] wherein the at least one interface uses at least one internal bus system, the at least one internal bus system including multiple lines [(see Figures 4, 5)] for [either] at least one of reading [or] and writing [(see Figure 9b, II-BUS, IO-BUS)].

7. (Amended) The bus system according to claim 2, [1, characterized in that the interfaces operate one or more internal bus systems which may comprise] wherein the at least one interface uses at least one internal bus system, the at least one internal bus system including multiple lines [(see Figures 4, 5) in hybrid operation according to claims 6 and 7] operating as a hybrid of multiple lines for reading and writing and multiple lines for at least one of reading and writing.

10. (Amended) The bus system according to claim 1, [characterized in that there is one] further comprising:

a register for managing and controlling the bus system [(EB-REG 0702, 0602)].

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~~10~~. (Amended) The bus system according to claim 1, [characterized in that] wherein the bus is controlled by a unit [(E-BUS MASTER)] which accesses a plurality of lower-level units [(E-BUS SLAVE)].

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~~11~~. (Amended) [The] A bus system [according to claim 1], comprising:

a plurality of at least one of individual lines, buses, and subbuses within at least one of a unit including at least one of a data flow processor (DFP), a field programmable gate array (FPGA), a dynamically programmable gate array (DPGA), and a unit having a multi-dimensional programmable cell architecture by means of which multiple units can be combined and/or memories and/or peripherals can be connected [(see Figure 10)], the plurality of the at least one of individual lines, buses and subbuses being bundled,

wherein the plurality of the at least one individual lines, buses and subbuses at least one of combines multiple units and connects at least one of memories and peripherals, and

[characterized in that the] wherein a bus control is transferred dynamically from one unit [(E-BUS MASTER)] to another [(MASTER record in EB-REG)].

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12. (Amended) The bus system according to claim ~~10~~, [1, characterized in that] wherein a lower-level unit [(E-BUS SLAVE) can request the] requests a bus control [(record of REQ-Master in EB-REG)].

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~~13~~. (Amended) The bus system according to claim 2, [1, characterized in that there is] further comprising:

a register indicating whether data [are] is stored in the at least one interface [interfaces (SET-REG, 0612, 0712)].

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~~14~~. (Amended) [The] A bus system [according to claim 1], comprising: [characterized in that the interfaces are either]

a plurality of at least one of individual lines, buses, and subbuses within at least one of a unit including at least one of a data flow processor (DFP), a field programmable gate array (FPGA), a dynamically programmable gate array (DPGA), and a unit having a multi-dimensional programmable cell architecture, the plurality of the at least one of individual lines, buses and subbuses being bundled,

wherein the plurality of the at least one individual lines, buses and subbuses at least one of combines multiple units and connects at least one of memories and peripherals,

wherein at least one interface combines the lines and creates the bus system, and

wherein the at least one interface is at least one of implemented directly on the unit [or are] and is created [by the] via a configuration of logic cells[, i.e., cells in DFP, FPGA, DPGA or similar units which fulfill simple logical or arithmetic functions according to their configuration].

18. (Amended) [The] A bus system [according to claim 1], comprising: [characterized in that the interfaces can be]

a plurality of at least one of individual lines, buses, and subbuses within at least one of a unit including at least one of a data flow processor (DFP), a field programmable gate array (FPGA), a dynamically programmable gate array (DPGA), and a unit having a multi-dimensional programmable cell architecture, the plurality of the at least one of individual lines, buses and subbuses being bundled,

wherein the plurality of the at least one individual lines, buses and subbuses at least one of combines multiple units and connects at least one of memories and peripherals,

wherein at least one interface combines the lines and creates the bus system, and

wherein the at least one interface is configured by at least one of a primary logic unit [and/or] and the unit itself [(see Figures 8, 11)].

16. (Amended) The bus system according to claim 15, [1, characterized in that]